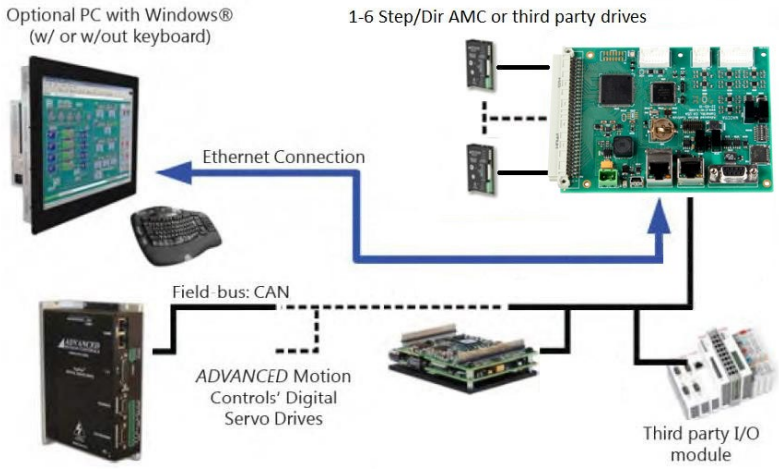
Description

The MACC11 (μMACC) is part of the *ADVANCED* Motion Controls® MACC controller family. It is designed to be a compact, low cost, controller for machine automation and/or process control applications. Based on firmware loaded, the MACC11 can control: up to 6 axes of servos or steppers via Pulse/Dir signals, servo drives via the CAN Bus, or 2 servo axes via PWM signals to digital servo drives. A typical system layout is shown below:



Click&Move®

Automation Solution

Applications are programmed in one of three ways depending on the firmware loaded:

- Using the powerful Click&Move® IDE (program resides on the PC)
- Directly in C by the user or *ADVANCED* Motion Controls® for custom projects (program resides on the MACC11)
- Click&Move® program on the MACC11 (future release)

When using a Click&Move® program running on a PC, the MACC11 communicates with the user application via the RS232, RS485, USB, or Ethernet ports. If programmed in C, the MACC11 can act as a stand-alone controller. Also, application specific pre-programmed MACC11 versions are available for OEMs. High speed hard real-time applications (e.g. servo loops, data acquisition, etc.) can be implemented in the user programmable MACC11 version.

Features

- C Programmable
- Compatible with Click&Move® IDE and HMI
- Micro SD Card
- Bicolor Status LED
- RTC with Battery Backup
- On-board I/O
  - 6 12-bit Analog Inputs
  - 2 11-bit Analog Outputs
  - 9 Digital I/O's
  - 8 DIP Switches

TECHNICAL SPECIFICATIONS

- 32-bit 120 MHz Risc Processor
- 256 kbyte zero wait state SRAM for data
- 1 Mbyte FLASH for firmware and user program storage
- 4 kbyte EEPROM for non-volatile parameter storage

INTERFACE CONNECTORS

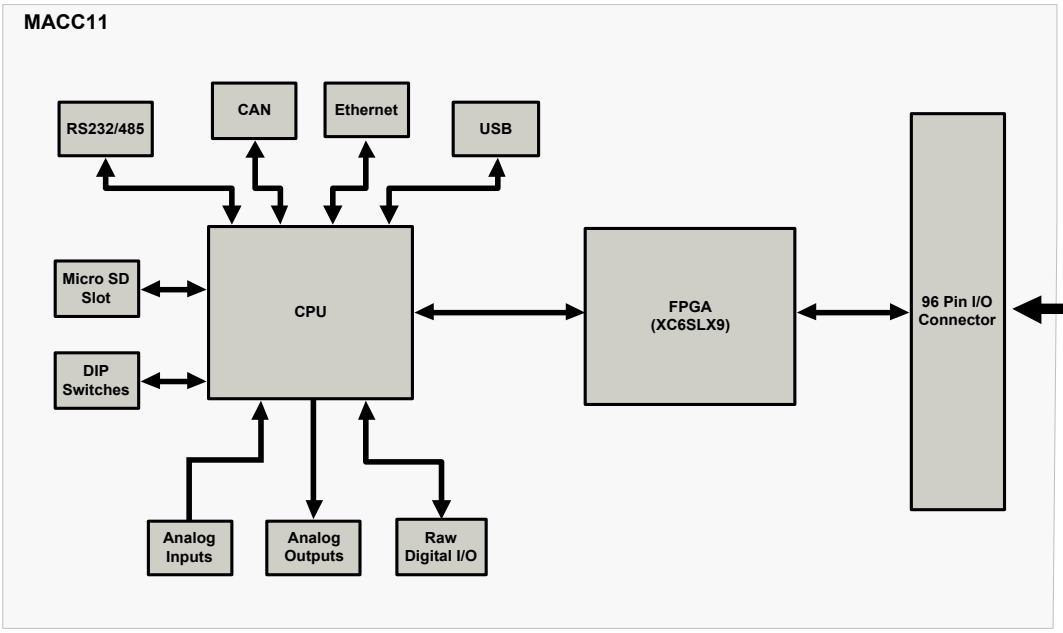
- 100 Mbit Ethernet
- USB 2.0 full speed (12 Mbit) peripheral (as mini USB connector) for firmware update purposes
- Isolated CAN Bus
- Isolated RS485/232

OPTIONAL I/O MODULES

Combine with the MACC11 for additional functionality:

MACCIO1	8 16-bit analog inputs
	8 16-bit analog outputs
	16 optocoupled digital inputs
	16 optocoupled digital outputs
	2x4 isolated high speed RS422 differential outputs
	4 isolated high speed RS422 differential inputs
	4 incremental or EnDat 2.0 encoder inputs (population option)
MACCIO2	16 optocoupled digital inputs
	16 optocoupled digital outputs
MACCIO3	6 stages for Step/Dir drive control (isolation population option)
	- 4 high speed RS422 differential outputs (per stage)
	- 2 high speed RS422 differential inputs (per stage)
	RS422 inputs for 4 incremental handwheels
	12 optocoupled digital inputs
	2 high speed optocoupled digital inputs
	12 optocoupled digital outputs
MACCIO4	4 stages for Step/Dir drive control
	RS422 inputs for 4 incremental handwheels
	4 digital inputs (per stage)
	4 digital outputs (per stage)

BLOCK DIAGRAM AND SPECIFICATIONS

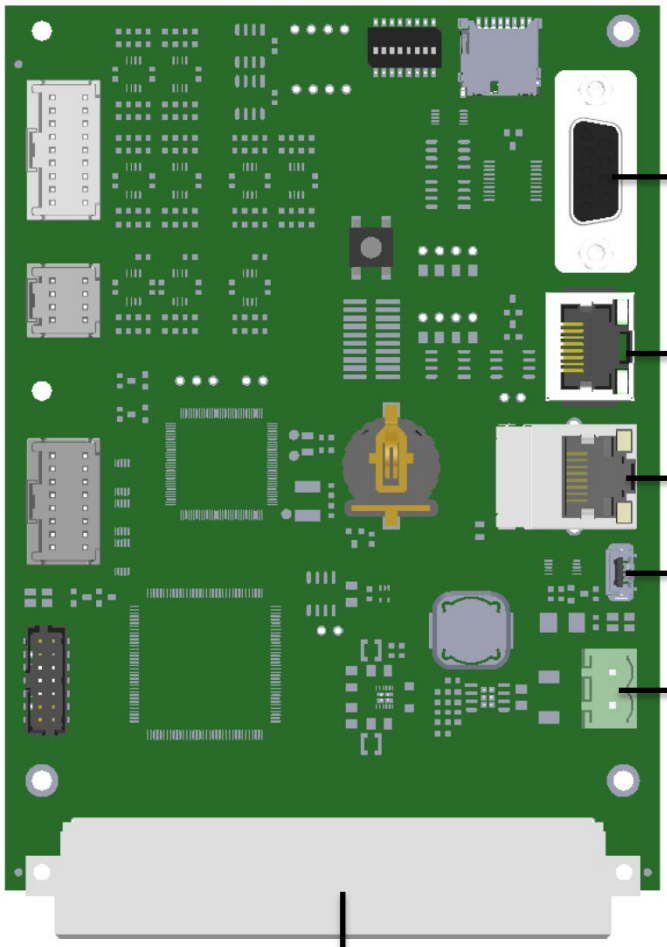


Power Specifications		
Description	Units	Value
DC Supply Voltage	VDC	24 (±25 %)
Power Consumption[1]	W	2.2
Control Specifications		
Description	Units	Value
Network Communication Interfaces	-	CANopen, RS232
Ethernet Connectivity	-	10 / 100 Mbps Ethernet with Auto MDI/MDIX
USB Connectivity	-	USB 2.0 (supports 12Mbps)
Number of Axes Supported	-	Field-bus and firmware dependent
Motors Supported	-	Closed Loop Vector, Single Phase (Brushed, Voice Coil, Inductive Load), Three Phase (Brushless)
CPU	-	TM4C1294NCPDT
CPU Clock	MHz	120
CPU on-chip FLASH	kB	1024
CPU on-chip RAM	kB	256
CPU Core	-	ARM Cortex-M4
FPGA	-	Xilinx® Spartan®-6 (XC6SLX9-2TQ144)
Mechanical Specifications		
Description	Units	Value
Agency Approvals	-	UL Pending, cUL Pending, CE Pending, RoHS II
Size (H x W x D)	mm (in)	142.30 x 99.95 x 18.10 (5.61 x 3.94 x 0.71)
Weight	g (oz)	113.4 (4.0)
Operating Temperature Range	°C (°F)	0 - 75 (32 - 167)
Storage Temperature Range	°C (°F)	-40 - 85 (-40 - 185)
ETHERNET COMM Connector	-	Shielded RJ-45 socket
USB 2.0 COMM Connector	-	5-pin, Mini USB B Type port
RS232 COMM Connector	-	9-pin, DSUB female
CANOPEN COMM Connector	-	Shielded RJ-45 socket
ANALOG INPUT Connector	-	18-pin, 2.00 mm spaced dual-row vertical header
ANALOG OUTPUT Connector	-	8-pin, 2.00 mm spaced dual-row vertical header
RAW DIGITAL I/O Connector	-	16-pin, 2.00 mm spaced dual-row vertical header
I/O Connector	-	96-pin, 2.54 mm spaced plug connector
POWER Connector	-	2-port, 5.08 mm spaced, enclosed, friction lock header

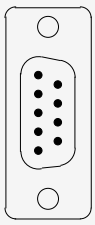
1. Measured in a full featured population option using firmware 1.0.0 in idle state

Information on Approvals and Compliances	
RoHS II Compliant	The RoHS II Directive 2011/65/EU restricts the use of certain substances including lead, mercury, cadmium, hexavalent chromium and halogenated flame retardants PBB and PBDE in electronic equipment.

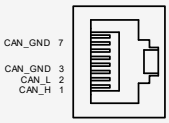
CONNECTOR INFORMATION



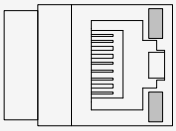
P1 – RS232/485 Communication Connector
- 9-pin DSUB female
- Mating connector (Tyco: Plug P/N 205204-4; Housing P/N: 5748677-1; Terminals P/N: 1658540-5 (loose) or 1658540-4 (strip)



P8 - CAN Connector
- Single RJ45 Plug
- Uses standard CAT 5e or CAT 6 Cable

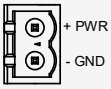


P11 - Ethernet Connector
- Single RJ45 Plug
- 10/100/1000 Mbps Ethernet with auto MDI/MDI-X
- Uses standard CAT 5e or CAT 6 Cable

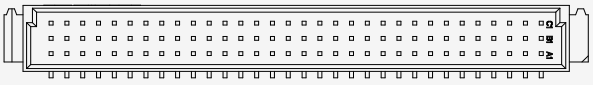


P3 - USB 2.0 Device Connector
- 5-pin, Mini USB B Type port
- Full (12 Mbps) speed
- Uses standard USB to MINI-B ASSY cable

P2 – Power Connector
- 2-pin, 5.08 mm spaced enclosed friction lock header
- 24 VDC Power Supply Connection
- Mating Connector Included (Phoenix Contact: P/N 1757019)

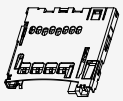


P12 - I/O Module Connector
- 96-pin, 2.54 mm spaced plug connector
- Optional external I/O Module interface

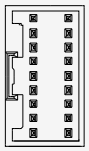


CONNECTOR INFORMATION (CONT.)

P28 - Micro SD Card Slots
- Standard removable SD card socket

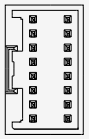


P6 – Analog Input Connector
- 18-pin, 2.00 mm spaced dual-row vertical header (Molex P/N 55917-1810)
- Mating Connector (Molex:P/N 51353-1800)



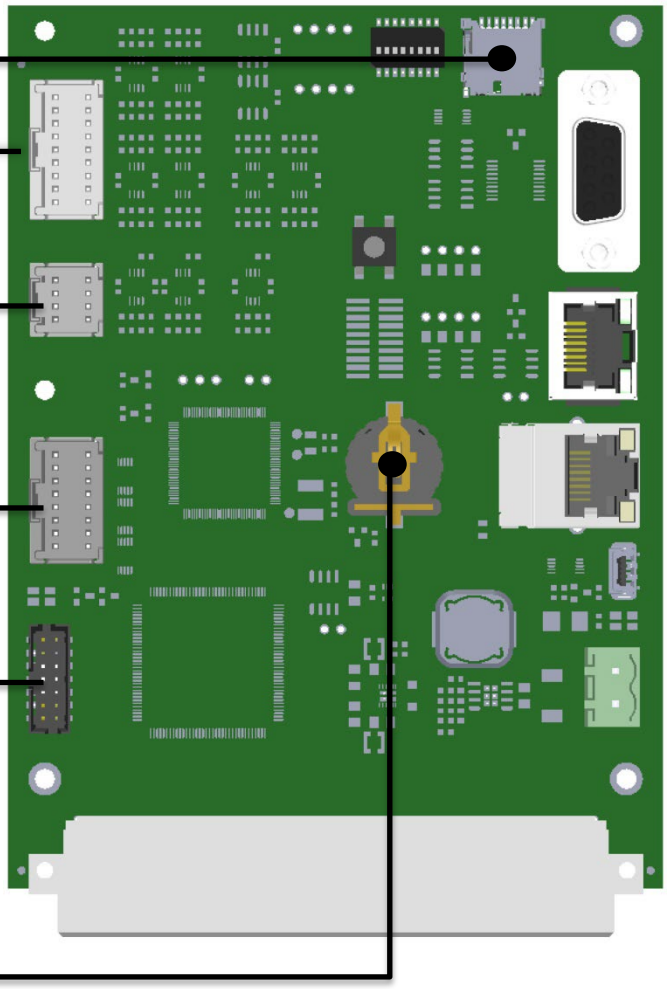
P7 – Analog Output Connector
- 8-pin, 2.00 mm spaced dual-row vertical header (Molex P/N 55917-0810)
- Mating Connector (Molex:P/N 51353-0800)

P4 – Raw Digital I/O Connectors
- 16-pin, 2.00 mm spaced dual-row vertical header (Molex P/N 55917-1610)
- Mating Connector (Molex:P/N 51353-1600)



P5 - JTAG1 - FPGA JTAG Connector
- 14-pin, dual row board-to-board header
- Connects to Standard Xilinx Platform Cable USB Ribbon Cable

Optional Real Time Clock Backup Battery Holder
- Holds a CR1220 (3V Lithium) battery



PIN FUNCTIONS

P1 - RS232/RS485 Communication Connector			
Pin	Name	Description / Notes	I/O
1	SELECT	RS232/485 selection. Pull to ground for RS485.	I
2	RS232 TX / RS485 TX-	Transmit Line (RS-232 or RS-485)	O
3	RS232 RX / RS485 RX-	Receive Line (RS-232 or RS-485)	I
4	RESERVED	Reserved	-
5	ISO GND	Isolated Signal Ground	IGND
6	RS485 TX+	Transmit Line (RS-485)	O
7	RESERVED	Reserved	-
8	RS485 RX+	Receive Line (RS-485)	I
9	RESERVED	Reserved	-

-RS232/485 TX CPU pin is 117
-RS232/485 RX CPU pin is 116
-RS485 DriveEnable CPU pin is 111
-RS485/232 selector signal can be read back at CPU pin 112

P2 - Power Connector			
Pin	Name	Description / Notes	I/O
1	GND	Power Supply Ground (Common with Analog and Digital Ground)	GND
2	PWR	Power Supply Input	I

P4 – Raw Digital I/O Connector*					
Pin	Name	Alternate	Description / Notes	I/O	CPU PIN
1	+3.3V**	-	+3.3V power supply for external circuits. Maximum load 150mA.	O	-
2	+5V	-	+5V power supply for external circuits. Maximum load 500mA.	O	-
3	GPIO1	AIN	General purpose digital I/O (Alt: analog input with 0-2.5V range)	I/O	12
4	GPIO2	AIN	General purpose digital I/O (Alt: analog input with 0-2.5V range)	I/O	13
5	GPIO3	AIN	General purpose digital I/O (Alt: analog input with 0-2.5V range)	I/O	14
6	GPIO4	SSI_CLK	General purpose digital I/O. Available only if FPGA bus signal ADDRESS12 is not used. (Alt: synchronous serial port clock signal)	I/O	5
7	GPIO5	SSI_FSS	General purpose digital I/O (Alt: synchronous serial port frame signal)	I/O	6
8	GPIO6	SSI_TX	General purpose digital I/O (Alt: synchronous serial port data transmit signal)	I/O	11
9	GPIO7	SSI_RX	General purpose digital I/O (Alt: synchronous serial port data receive signal)	I/O	27
10	GPIO8	AIN, I2C_SCL	General purpose digital I/O (Alt: analog input with 0-2.5V range / I2C bus clock signal)	I/O	121
11	GPIO9	AIN, I2C_SDA	General purpose digital I/O (Alt: analog input with 0-2.5V range / I2C bus data signal)	I/O	120
12	GPIO10	ENC_A	General purpose digital I/O. Available only if FPGA bus signal ADDRESS9 is not used. (Alt: quadrature encoder A signal)	I/O	82
13	GPIO11	ENC_B	General purpose digital I/O. Available only if FPGA bus signal ADDRESS10 is not used. (Alt: quadrature encoder B signal)	I/O	83
14	GPIO12	ENC_I	General purpose digital I/O. Available only if FPGA bus signal ADDRESS11 is not used. (Alt: quadrature encoder index signal)	I/O	84
15	DIGITAL GROUND	-	Digital Ground	DGND	-
16	DIGITAL GROUND	-	Digital Ground	DGND	-

*GPIO functions, direction and/or alternate function are firmware programmable.
**Digital I/O logic level is 3.3V

P6 – Analog Input Connector*				
Pin	Name	Description / Notes	I/O	CPU PIN
1	ANALOG_IN_1-	Differential analog inverted input. For single-ended use, connect to analog ground.	I	-
2	ANALOG_IN_2-	Differential analog inverted input. For single-ended use, connect to analog ground.	I	-
3	ANALOG_IN_1+	Differential analog non-inverted input	I	128
4	ANALOG_IN_2+	Differential analog non-inverted input	I	127
5	ANALOG GROUND	Analog ground	AGND	-
6	ANALOG GROUND	Analog ground	AGND	-
7	ANALOG_IN_3-	Differential analog inverted input. For single-ended use, connect to analog ground.	I	-
8	ANALOG_IN_4-	Differential analog inverted input. For single-ended use, connect to analog ground.	I	-
9	ANALOG_IN_3+	Differential analog non-inverted input	I	126
10	ANALOG_IN_4+	Differential analog non-inverted input	I	125
11	ANALOG GROUND	Analog ground	AGND	-
12	ANALOG GROUND	Analog ground	AGND	-
13	ANALOG_IN_5-	Differential analog inverted input. For single-ended use, connect to analog ground.	I	-
14	ANALOG_IN_6-	Differential analog inverted input. For single-ended use, connect to analog ground.	I	-
15	ANALOG_IN_5+	Differential analog non-inverted input	I	124
16	ANALOG_IN_6+	Differential analog non-inverted input	I	123
17	ANALOG GROUND	Analog ground	AGND	-
18	ANALOG GROUND	Analog ground	AGND	-

*Analog inputs have a default range of ±10V. Resolution is 12-bit. Sampling rate is firmware dependent.

P7 – Analog Output Connector*			
Pin	Name	Description / Notes	I/O
1	ANALOG_OUT_1	Single-ended analog output	O
2	ANALOG_OUT_2	Single-ended analog output	O
3	ANALOG GROUND	Analog ground	AGND
4	ANALOG GROUND	Analog ground	AGND
5	ANALOG_OUT_3	Optional single-ended analog output. Available only if FPGA bus signals ADDRESS2 and ADDRESS3 are not used.	O
6	-12V	Negative power supply for external circuits. Maximum load 20mA.	O
7	ANALOG GROUND	Analog ground	AGND
8	+12V	Positive power supply for external circuits. Maximum load 20mA.	O

-ANALOG_OUT_1 is CPU pin 42 and 43 configured as PWM Outputs
-ANALOG_OUT_2 is CPU pin 44 and 45 configured as PWM Outputs
-ANALOG_OUT_3 is CPU pin 49 and 50 configured as PWM Outputs
*Analog outputs have a default range of ±10V. Settling time and resolution are firmware dependent parameters. These analog signals are the result of low pass filtering PWM signals using a 3rd order Chebyshev filter with a 3.5 kHz cut-off frequency.

HARDWARE SETTINGS

Switch Functions

Switch	Description
BTN500	Hardware Reset - automatic system reboot.

Switch	Description
SW400	8-position user-defined DIP Switch (firmware dependent functions)

LED Functions

LED	Description
LED100	Status Bi-color LED (firmware dependent functions).
LED2	Power Supply Bi-color LED. Red LED indicates the internal +5V power supply is operational. Green LED indicates that the system reset signal is inactive, and the system is running.

Jumper Settings

Jumper	Description	Configuration	
	Header Jumper	Not Installed*	Installed
JF600	CAN1 bus termination.	Non-terminating node	Terminating node
JF100	Boot Select	Standard Operation	Stay in boot loader after reset

*Default

CAN Connector LED Functions

LED	Description
Yellow	Displays the dominant bits (traffic) on the bus
Green	Displays the traffic generated by the µMACC

FPGA I/O INFORMATION

Main FPGA I/O Connector Pinout

Note that the pin labels on the silkscreen correspond to the connector labels as such:
Pins 1-32 = C1-C32; Pins 33-64 = B1-B32; Pins 65-96 = A1-A32

P12 – I/O Connector

Pin	Description/Notes	FPGA Pin	Pin	Description/Notes	FPGA Pin	Pin	Description/Notes	FPGA Pin
1	I/O	143	33	I/O	142	65	+POWER_IN	-
2	I/O	141	34	I/O	140	66	+POWER_IN	-
3	I/O	139	35	I/O	138	67	+POWER_IN	-
4	I/O	137	36	I/O	134	68	GND	-
5	I/O	133	37	I/O	132	69	GND	-
6	I/O	131	38	I/O	127	70	I/O	126
7	I/O	124	39	I/O	123	71	I/O	121
8	I/O	120	40	I/O	119	72	I/O	118
9	I/O	117	41	I/O	116	73	I/O	115
10	I/O	114	42	I/O	112	74	I/O	111
11	I/O	38	43	I/O	40	75	I/O	41
12	I/O	43	44	I/O	44	76	NC	-
13	I/O	45	45	I/O	46	77	GND	-
14	I/O	47	46	I/O	48	78	GND	-
15	I/O	50	47	I/O	51	79	GND	-
16	I/O	55	48	I/O	56	80	GND	-
17	I/O	57	49	I/O	58	81	GND	-
18	I/O	59	50	I/O	61	82*	I2C_SCL	-
19	I/O	62	51	I/O	64	83*	I2C_SDA	-
20	I/O	66	52	I/O	67	84	RESET	-
21	I/O	105	53	I/O	104	85	GND	-
22	I/O	102	54	I/O	101	86	GND	-
23	I/O	100	55	I/O	99	87	+3.3V	-
24	I/O	98	56	I/O	97	88	+3.3V	-
25	I/O	95	57	I/O	94	89	GND	-
26	I/O	93	58	I/O	92	90	GND	-
27	I/O	88	59	I/O	87	91	+3.3V	-
28	I/O	85	60	I/O	84	92	+3.3V	-
29	I/O	83	61	I/O	82	93	GND	-
30	I/O	81	62	I/O	80	94	GND	-
31	I/O	79	63	I/O	78	95	+5V	-
32	I/O	75	64	I/O	74	96	+5V	-

*P12.82 and P12.83 forms an I²C bus. The CPU is the I²C master. CPU pins: 61, 60

Additional FPGA Signals

Certain FPGA pins have predefined functionality. Configure these pins according to the following table.

Signal	FPGA Pin	CPU Pin	Dir[1]	Functionality
FPGA_STATUS	35	105	I/O	General Purpose signal between the CPU and the FPGA
SYS_CLK	15	102	I	Master clock input. Note 2.
FPGA_CFG_PRG	37	3	I	FPGA serial programming interface.
FPGA_CFG_CLK	70	4	I	FPGA serial programming interface.
FPGA_CFG_DATA	65	2	I	FPGA serial programming interface.
FPGA_CFG_INIT	39	86	I/O	FPGA serial programming interface.
FPGA_CFG_DONE	71	74	O	FPGA serial programming interface.

Note 1: All direction information is from the FPGA point of view.

Note 2: The frequency of this CPU clock output is software programmable.

FPGA Auxiliary Power Supply

The auxiliary power supply of the FPGA is 3.3V. The following line must be specified in the UCF file of the FPGA project to indicate this fact to the compiler:

CONFIG VCCAUX=3.3;

For more information refer to the "Supply Voltages for the IOBs" section of the UG381 User's Guide from Xilinx. (http://www.xilinx.com/support/documentation/user_guides/ug381.pdf)

Bitfile Generation for Slave Serial Download

Change the default configuration startup clock setting from JTAGCLK to CCLK. Make sure to have this line in the *etc\bitgen.ut* file of the Xilinx EDK project:

-g StartUpClk:CCLK

CPU External Interface Module Signals

This is the primary interface between the CPU and the FPGA. It is a synchronous bus, with 8 data and 13 address lines.

Signal	FPGA Pin	CPU Pin	Dir[1]	Functionality
BUS_CLK	14	62	I	Bus clock. Active only during bus transactions. The frequency is programmable.
RD	1	103	I	Active high read signal.
WR	2	92	I	Active high write signal
DATA0	5	18	I/O	Data signal.
DATA1	6	19	I/O	Data signal.
DATA2	7	20	I/O	Data signal.
DATA3	8	21	I/O	Data signal.
DATA4	9	22	I/O	Data signal.
DATA5	10	23	I/O	Data signal.
DATA6	11	24	I/O	Data signal.
DATA7	12	25	I/O	Data signal.
ADDRESS0	16	40	I	Address signal.
ADDRESS1	17	41	I	Address signal.
ADDRESS2	21	50	I	Address signal.
ADDRESS3	22	49	I	Address signal.
ADDRESS4	23	75	I	Address signal.
ADDRESS5	24	76	I	Address signal.
ADDRESS6	26	77	I	Address signal.
ADDRESS7	27	78	I	Address signal.
ADDRESS8	29	81	I	Address signal.
ADDRESS9	30	82	I	Address signal.
ADDRESS10	32	83	I	Address signal.
ADDRESS11	33	84	I	Address signal.
ADDRESS12	34	5	I	Address signal.

Note 1: All direction information is from the FPGA point of view.

FPGA JTAG Connector

Contains the JTAG signals of the FPGA. The connector is the standard 2mm header that the Xilinx Platform Cable USB JTAG device uses. The standard ribbon cable of the Xilinx device can be used to connect to the MACC11 board.

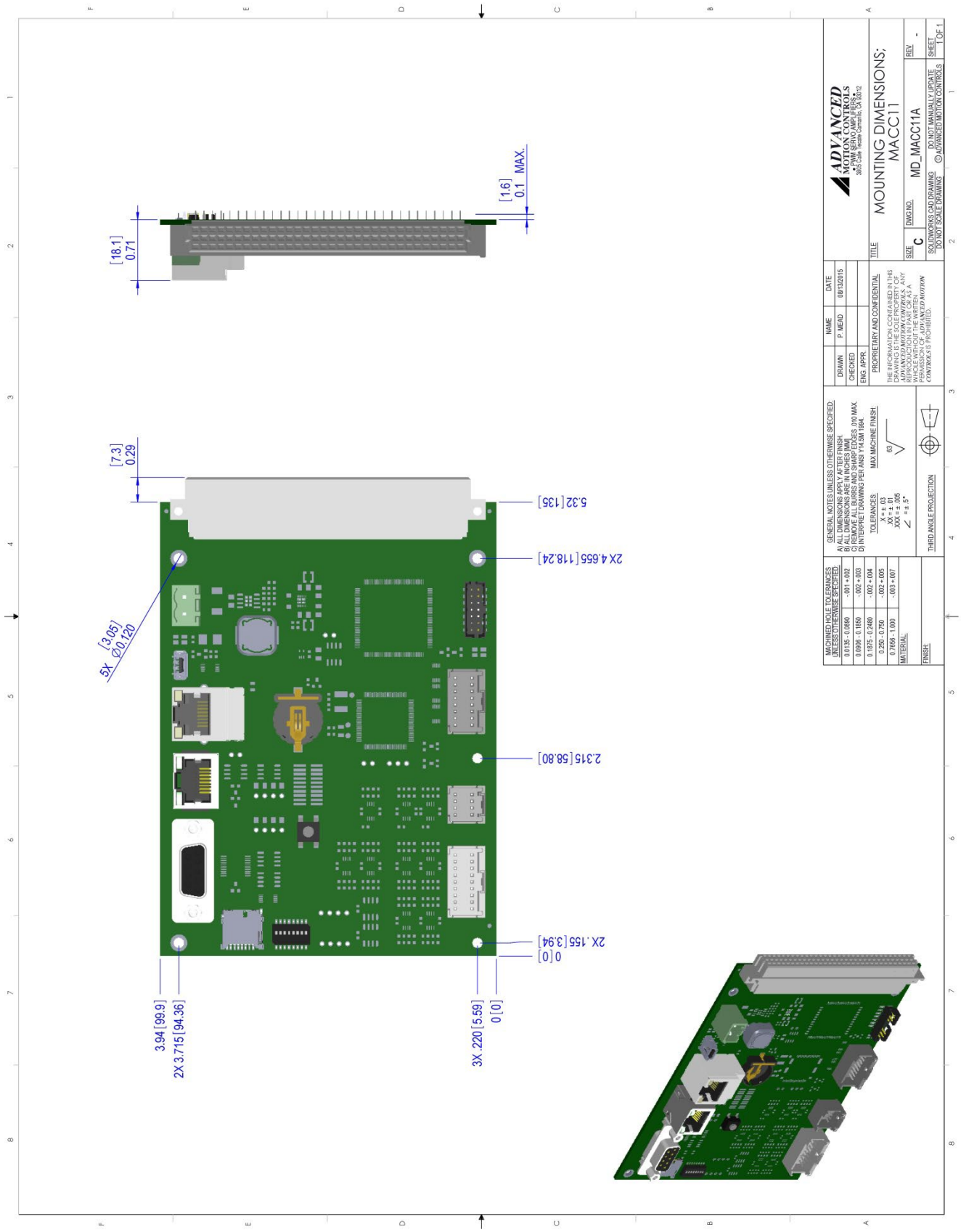
P5 – FPGA JTAG Connector

Pin	Name	Description	Dir
1	GND	Ground	-
2	+3.3V	+3.3V power supply for the external JTAG master	O
3	GND	Ground	-
4	TMS	Test mode select	I
5	GND	Ground	-
6	TCK	Test clock	I
7	GND	Ground	-
8	TDO	Test data output	O
9	GND	Ground	-
10	TDI	Test data input	I
11	GND	Ground	-
12	NC	Not connected	-
13	GND	Ground	-
14	NC	Not connected	-

Firmware Updates

Contact *ADVANCED* Motion Controls for new firmware and firmware update software.

MOUNTING DIMENSIONS

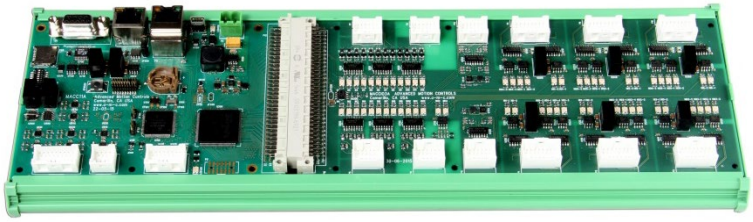


APPENDIX A: FIRMWARE DESCRIPTION

Firmware Version	Description
MACC11_1.0.x	6 axes PVT to Step/Dir motion controller using the MACCIO3 extension board
MACC11_1.1.x	4 axes PVT to Step/Dir motion controller using the MACCIO4 extension board

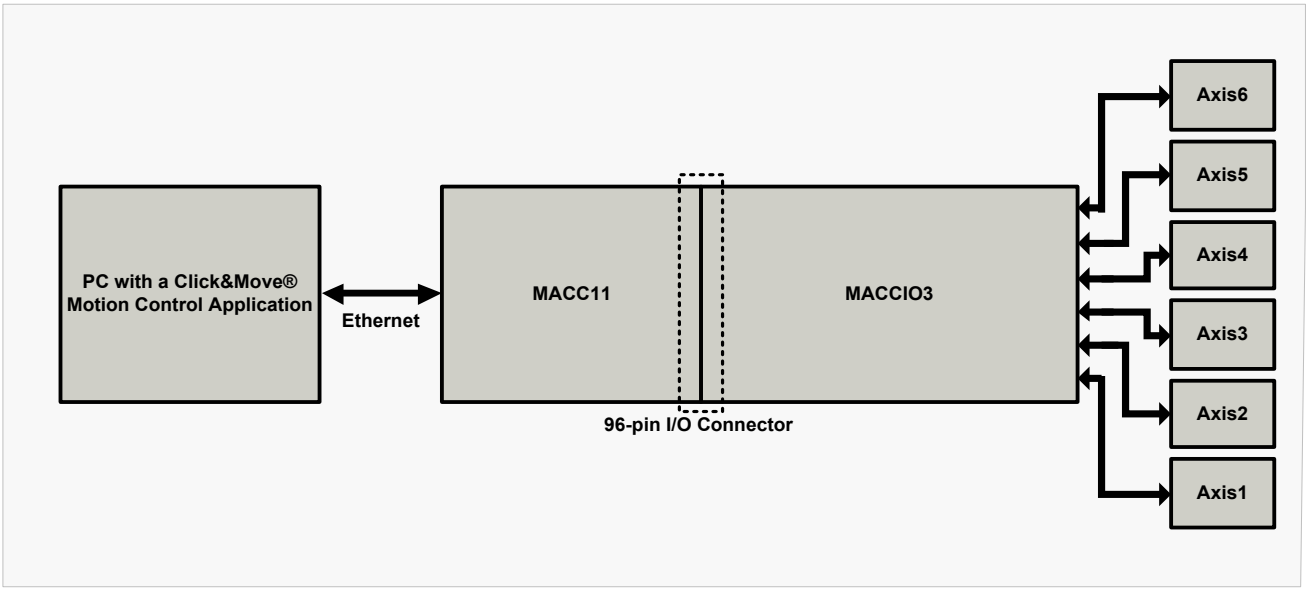
MACC11_1.0.2

This appendix contains information on the MACC11_1.0.2 firmware. It is compatible with the MACCIO3 I/O expansion module. For more information on the MACCIO3, refer to the "MACCIO Extension Boards" document. The primary function of the MACCIO3 is to allow support of position mode drives or stepper (open or closed loop configuration) using Step/Dir or PWM/Dir target position input with available Click&Move resources.



With this firmware, the MACC11 converts interpolated position target signals to Step/Dir or PWM/Dir signals in real time. From the motion control application point of view, the MACC11 acts as 6 independent CANopen based servo drives, featuring 6 independent CANopen object dictionaries including all the necessary CAN objects to simulate the functionality of 6 position mode servos. *ADVANCED* Motion Controls' analog and digital I/O are emulated as well, allowing the user access to the I/O resources of the MACCIO3 board. The Click&Move application can access the MACC11 using the Ethernet interface. The CanAdaptorEnetUdp CAN device option of the CAN_CHANNEL C&M function block encapsulates the CAN messages into UDP/IP frames that are decoded by the MACC11. The integrated PVT to discrete position algorithm uses the PVT points sent by the motion control application to generate an interpolated target position signal at 100µs update rate. The maximum pulse frequency is 1µs. The PWM frequency in PWM/Dir mode can be set between 100 Hz and 25500 Hz. The (CAN) device addresses of the emulated axes are constant (1 – 6). The IP address of the device and numerous other firmware parameters can be modified using a configuration tool.

A typical system setup is shown below:



MACCIO3 Specifications

Mechanical Specifications		
Description	Units	Value
Size (H x W x D) [including MACC11]	mm (in)	363.25 x 99.95 x 18.10 (14.30 x 3.94 x 0.71)
Weight [including MACC11]	g (oz)	240.97 (8.5)
Operating Temperature Range	°C (°F)	0 - 75 (32 - 167)
Storage Temperature Range	°C (°F)	-40 - 85 (-40 - 185)
P1, P2, P3, P4, P9, P10 Motion Control Interface Connectors	-	16-pin, 2.00 mm spaced dual-row vertical header (Mating Connector Molex: 51353-1600)
P5, P6 Isolated Digital Inputs Connectors	-	12-pin, 2.00 mm spaced dual-row vertical header (Mating Connector Molex: 51353-1200)
P7, P8 Isolated Digital Outputs Connectors	-	12-pin, 2.00 mm spaced dual-row vertical header (Mating Connector Molex: 51353-1200)
P11, P12 Encoder Connectors	-	12-pin, 2.00 mm spaced dual-row vertical header (Mating Connector Molex: 51353-1200)

MACCIO3 Pin Functions

P1, P2, P3, P4, P9, P10 – Motion Control Interface Connectors*				
Pin	Name	MACCIO3 Name	Description / Notes	I/O
1	DIGITAL GROUND	HSIOx_GND	Digital Ground.	DGND
2	DIGITAL GROUND	HSIOx_GND	Digital Ground.	DGND
3	TRIGGER_AT_VALUE+	HSOUTx_4+	See Motion Control Interface Pin Details below	O
4	DIR+	HSOUTx_2+	See Motion Control Interface Pin Details below	O
5	TRIGGER_AT_VALUE-	HSOUTx_4-	See Motion Control Interface Pin Details below	O
6	DIR-	HSOUTx_2-	See Motion Control Interface Pin Details below	O
7	DIGITAL GROUND	HSIOx_GND	Digital Ground.	DGND
8	DIGITAL GROUND	HSIOx_GND	Digital Ground.	DGND
9	ENABLE+	HSOUTx_3+	See Motion Control Interface Pin Details below	O
10	STEP+ / PWM+	HSOUTx_1+	See Motion Control Interface Pin Details below	O
11	ENABLE-	HSOUTx_3-	See Motion Control Interface Pin Details below	O
12	STEP- / PWM-	HSOUTx_1-	See Motion Control Interface Pin Details below	O
13	CAPTURE+	HSINx_2+	See Motion Control Interface Pin Details below	I
14	FAULT+	HSINx_1+	See Motion Control Interface Pin Details below	I
15	CAPTURE-	HSINx_2-	(Leave open for single-ended signals) See Motion Control Interface Pin Details below	I
16	FAULT-	HSINx_1-	(Leave open for single-ended signals) See Motion Control Interface Pin Details below	I

*P1 = Axis1; P2 = Axis2; P3 = Axis3; P4 = Axis4; P9 = Axis5; P10 = Axis6

Motion Control Interface Pin Details

All signals of the motion control hardware interface are RS422 differential (by default these signals have galvanic isolation; a non-isolated version of the MACCIO3 is also available.) The hardware interface to the position mode drives or steppers contains the following signals:

Signal	Description
Step Output	Every pulse on this output increments/decrements the position counter of the positioning device.
PWM Output	When PWM/Dir output mode has been selected, this is the PWM signal output.
Dir Output	Direction signal for the device. The level of this signal indicates if the position counter should be incremented or decremented at every Step pulse.
Enable Output	Enables or Disables the device.
TriggerAtValue Output	Programmable firmware function. A comparator implemented in the FPGA can be set up to compare some selectable internal signals (available inside the FPGA) of the emulated drive. The TriggerAtValue Output indicates when the preset value and the signal are the same. The use of this signal is application specific.
Ready or Fault Input	Indicates the internal status of the positioning device. When active (or inactive if the polarity is inverted) the status word of the emulated servo drive will indicate a “Drive Internal Error” to the motion control application. Default polarity is INVERTED, meaning by default the input acts as a Ready status indicator
Capture Input	Selectable signals from the emulated drive can be captured using the selected edge of the Capture Input. Only signals that are accessible inside the FPGA can be captured. This can be used as a home switch input, capturing the actual position (always equal to the target position in the MACC11) during the homing procedure.

The MACCIO3 board features additional general purpose I/Os that can be used for application specific purposes (i.e. limit switch inputs). The MACCIO3 also has support for up to four quadrature encoder inputs. These signals can be used as the position signal source or handwheels.

P5 – Isolated Digital Inputs Connector			
Pin	Name	Description / Notes	I/O
1	GND_ISOIN_B	Input common for ISOIN_5…ISOIN_8	-
2	GND_ISOIN_A	Input common for ISOIN_1…ISOIN_4	-
3	ISOIN_8	Isolated digital input	I
4	ISOIN_4	Isolated digital input	I
5	ISOIN_7	Isolated digital input	I
6	ISOIN_3	Isolated digital input	I
7	GND_ISOIN_B	Input common for ISOIN_5…ISOIN_8	-
8	GND_ISOIN_A	Input common for ISOIN_1…ISOIN_4	-
9	ISOIN_6	Isolated digital input	I
10	ISOIN_2	Isolated digital input	I
11	ISOIN_5	Isolated digital input	I
12	ISOIN_1	Isolated digital input	I

P6 – Isolated Digital Inputs Connector			
Pin	Name	Description / Notes	I/O
1	NC	Not Connected	-
2	GND_ISOIN_C	Input common for ISOIN_9…ISOIN_12	-
3	ISOIN_14-	Isolated differential digital input negative terminal	I
4	ISOIN_12	Isolated digital input	I
5	ISOIN_14+	Isolated differential digital input positive terminal	I
6	ISOIN_11	Isolated digital input	I
7	NC	Not Connected	-
8	GND_ISOIN_C	Input common for ISOIN_9…ISOIN_12	-
9	ISOIN_13-	Isolated differential digital input negative terminal	I
10	ISOIN_10	Isolated digital input	I
11	ISOIN_13+	Isolated differential digital input positive terminal	I
12	ISOIN_9	Isolated digital input	I

P7 – Isolated Digital Outputs Connector			
Pin	Name	Description / Notes	I/O
1	GND_ISOOUT_B	Digital output common for ISOOUT_5…ISOOUT_8	-
2	GND_ISOOUT_A	Digital output common for ISOOUT_1…ISOOUT_4	-
3	ISOOUT_8	Isolated digital output	O
4	ISOOUT_4	Isolated digital output	O
5	ISOOUT_7	Isolated digital output	O
6	ISOOUT_3	Isolated digital output	O
7	ISOOUT_B	Digital output pull-up for ISOOUT_5…ISOOUT_8	-
8	ISOOUT_A	Digital output pull-up for ISOOUT_1…ISOOUT_4	-
9	ISOOUT_6	Isolated digital output	O
10	ISOOUT_2	Isolated digital output	O
11	ISOOUT_5	Isolated digital output	O
12	ISOOUT_1	Isolated digital output	O

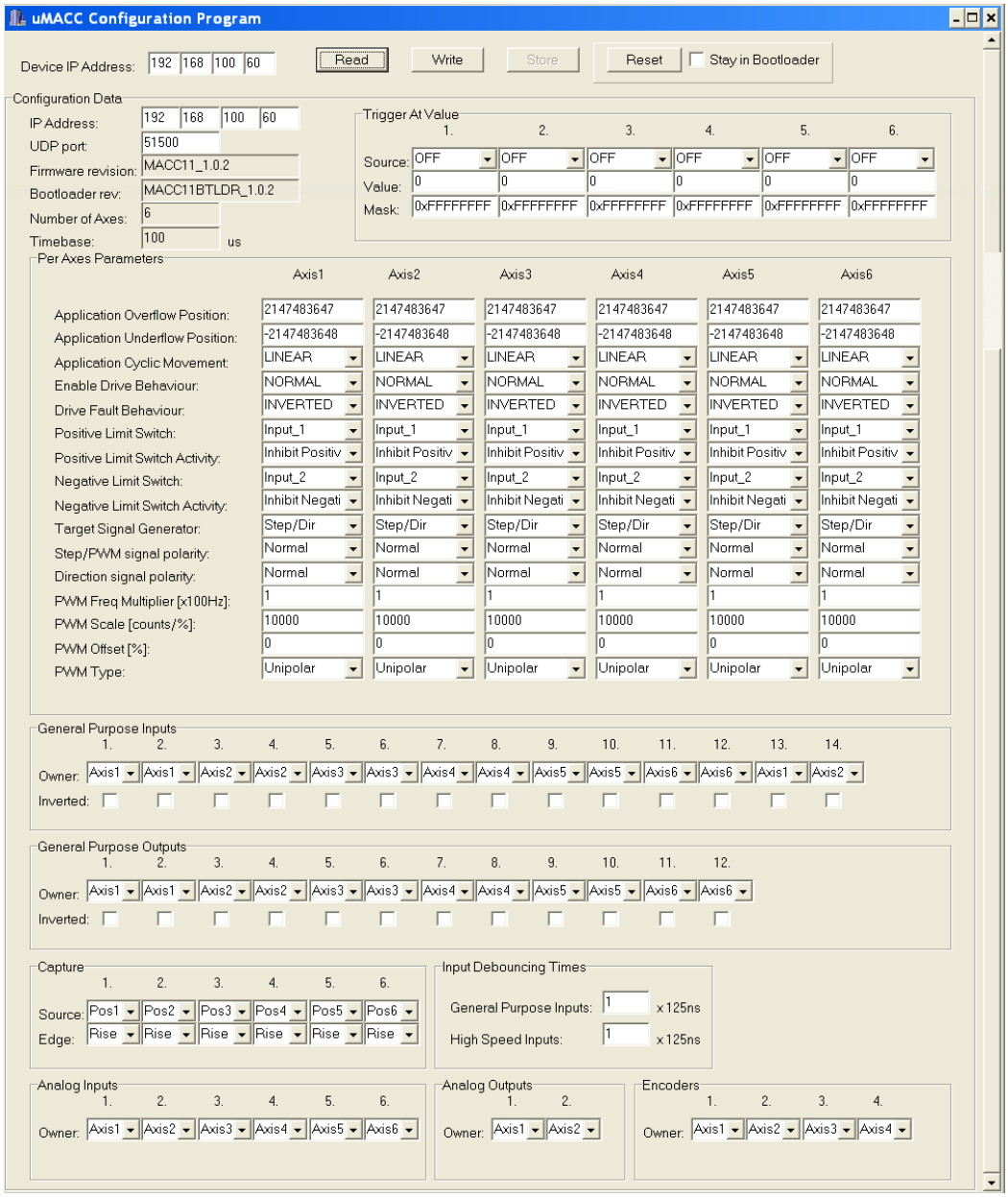
P8 – Isolated Digital Outputs Connector			
Pin	Name	Description / Notes	I/O
1	NC	Not Connected	-
2	GND_ISOOUT_C	Digital output common for ISOOUT_9…ISOOUT_12	-
3	NC	Not Connected	-
4	ISOOUT_12	Isolated digital output	O
5	NC	Not Connected	-
6	ISOOUT_11	Isolated digital output	O
7	NC	Not Connected	-
8	ISOOUT_C	Digital output pull-up for ISOOUT_9…ISOOUT_12	-
9	NC	Not Connected	-
10	ISOOUT_10	Isolated digital output	O
11	NC	Not Connected	-
12	ISOOUT_9	Isolated digital output	O

P11 – Encoder Connector			
Pin	Name	Description / Notes	I/O
1	GROUND	Ground	GND
2	GROUND	Ground	GND
3	ENC_B_2-	Differential encoder 2 B-channel negative input (leave open for single-ended encoders)	I
4	ENC_B_1-	Differential encoder 1 B-channel negative input (leave open for single-ended encoders)	I
5	ENC_B_2+	Differential encoder 2 B-channel positive input	I
6	ENC_B_1+	Differential encoder 1 B-channel positive input	I
7	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
8	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
9	ENC_A_2-	Differential encoder 2 A-channel negative input (leave open for single-ended encoders)	I
10	ENC_A_1-	Differential encoder 1 A-channel negative input (leave open for single-ended encoders)	I
11	ENC_A_2+	Differential encoder 2 A-channel positive input	I
12	ENC_A_1+	Differential encoder 1 A-channel positive input	I

P12 – Encoder Connector			
Pin	Name	Description / Notes	I/O
1	GROUND	Ground	GND
2	GROUND	Ground	GND
3	ENC_B_4-	Differential encoder 4 B-channel negative input (leave open for single-ended encoders)	I
4	ENC_B_3-	Differential encoder 3 B-channel negative input (leave open for single-ended encoders)	I
5	ENC_B_4+	Differential encoder 4 B-channel positive input	I
6	ENC_B_3+	Differential encoder 3 B-channel positive input	I
7	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
8	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
9	ENC_A_4-	Differential encoder 4 A-channel negative input (leave open for single-ended encoders)	I
10	ENC_A_3-	Differential encoder 3 A-channel negative input (leave open for single-ended encoders)	I
11	ENC_A_4+	Differential encoder 4 A-channel positive input	I
12	ENC_A_3+	Differential encoder 3 A-channel positive input	I

Configuration Program

The MACC11 configuration program can be used to configure certain device parameters.



By default, all fields are empty when starting the program.

To successfully use the configuration program, follow the procedure outlined below.

1. Set the **IP Address of the Ethernet device on the host PC** to **192.168.100.1**. (Note that the last byte can be anything other than the last byte of the IP Address of the MACC11). Set the **Network Mask** to **255.255.255.0**.
2. Connect the MACC11 to the PC using an Ethernet cable.
3. Start the Configuration Program.
4. The MACC11 has a default IP Address of **192.168.100.60**. Enter this into the *Device IP Address* field.
5. After applying power to the MACC11, click the *Read* button. This will populate the configuration fields with the current configuration data.
6. Once the configuration fields have been appropriately modified (see table below), click the *Write* button to download the new settings into the MACC11.
7. Click the *Store* button to store the new settings into non-volatile memory.
8. Click the *Reset* button to reset the MACC11. New settings will not be available until a device reset has been performed. Note that if the *Stay in Bootloader* box is checked, the MACC11 will remain in Bootloader mode waiting for firmware download.

Configuration Program Fields		
Panel	Field	Description
Configuration Data	IP Address / UDP Port	Configure the IP Address, and UDP Port the MACC11 uses for UDP based communication with the motion control application
Trigger At Value	Source / Value / Mask	Configure the comparator section of the device. 6 independent identical channels have a dedicated output to indicate the status. See the 'Motion Control Interface' connector pinout for the digital outputs. Each comparator can compare the *Value* to one of the following *Sources*: - ActualPosition of Axes 1-6 - Encoder 1 counter - Encoder 2 counter - Encoder 3 counter - Encoder 4 counter - Isolated Digital Inputs represented as an integer value The *Mask* values are applied to both the specified compare value and the signal it is being compared to, reducing the active range of comparation. A linear counting of the encoder counter or ActualPosition counter can be turned into a cyclic pulse output in this way.
Per Axes Parameters	Application Overflow Position	Software position limit. Use the default value in linear mode. Sets the single turn resolution in rotary mode.
	Application Underflow Position	Software position limit. Use the default value in linear mode. Set to zero in rotary mode.
	Application Cyclic Movement	Configures each Axis as Linear or Rotary.
	Enable Drive Behavior	Controls the polarity of the Enable Digital Output signal (NORMAL, INVERTED, constant ON, or constant OFF)
	Drive Fault Behavior	Controls the polarity of the Fault Digital Input signal (NORMAL, INVERTED, OFF). Default is INVERTED.
	Positive Limit Switch	Selects which general purpose input of the axis is to be used as a positive limit switch.
	Positive Limit Switch Activity	Select one available activity. Inhibit positive motion will let the axis move in only the negative direction when the positive limit switch is active.
	Negative Limit Switch	Selects which general purpose input of the axis is to be used as a negative limit switch.
	Negative Limit Switch Activity	Select one available activity. Inhibit negative motion will let the axis move in only the positive direction when the negative limit switch is active.
	Target Signal Generator	Select Step/Dir or PWM/Dir as the target signal.
	Step/PWM Signal Polarity	Changes the Step or PWM hardware signal polarity. In PWM mode, inverting this signal means inverting the direction of the motion.
	Direction Signal Polarity	Changes the Dir hardware signal polarity.
	PWM Freq Multiplier [x100Hz]	Sets the PWM frequency in PWM mode. The resolution is 100 Hz. The maximum frequency is 25500 Hz (e.g. a value from 1 to 255).
	PWM Scale [counts%]	Sets the resolution of the PWM signal. This is the scale factor between the internal position counter and the PWM signal. For example, when 10000 has been set, it means that 10000 counts change in the position will change the pulse width by 1%.
	PWM Offset [%]	Sets a constant offset for the PWM signal. This is the pulse width at zero position for Unipolar type of PWM.
	PWM Type	Bipolar type means that at zero position, the pulse width is (50% + PWM Offset). In this case, when the position counter gets into the negative region, the pulse width becomes less than this. When the position counter gets into the positive region, the pulse width becomes more than this. The Dir signal is operational in this case as well, however it is not necessarily used. Unipolar type means that at zero position, the pulse width is (PWM Offset). When the position counter gets into the negative region, the pulse width starts to increase again. Use the Dir signal to show the position direction to the controlled device.

Note: If SW8 of DIP Switch SW400 is ON during power-up, the default firmware parameters will be loaded.

Configuration Program Fields (continued)		
Panel	Field	Description
General Purpose Inputs	Owner / Inverted	*Owner* selects which Axis controls each input. The *Inverted* checkbox changes the polarity of the signal.
General Purpose Outputs	Owner / Inverted	*Owner* selects which Axis controls each output. The *Inverted* checkbox changes the polarity of the signal.
Capture	Source / Edge	Select the signal *Source* to be captured: - ActualPosition of Axes 1-6 - Encoder 1 counter - Encoder 2 counter - Encoder 3 counter - Encoder 4 counter - Isolated Digital Inputs represented as an integer value Select the *Edge* of the signal to trigger on (Rise, Fall, Both). If OFF is selected, that Capture module is turned off.
Encoders	Owner	*Owner* selects which Axis controls each encoder input.
Analog Inputs	Owner	*Owner* selects which Axis controls each input. Analog inputs reside on the MACC11 board.
Analog Outputs	Owner	*Owner* selects which Axis controls each output. Analog outputs reside on the MACC11 board.
Input Debouncing Times	General Purpose and High Speed Inputs	Sets the hardware debouncing time for both the General Purpose and High Speed Inputs. Resolution is 125ns. High Speed Inputs are the dedicated Capture Inputs and dedicated Fault Inputs.

Status Indicators

The table below describes the behavior of the bicolor status and error indicator LED100.

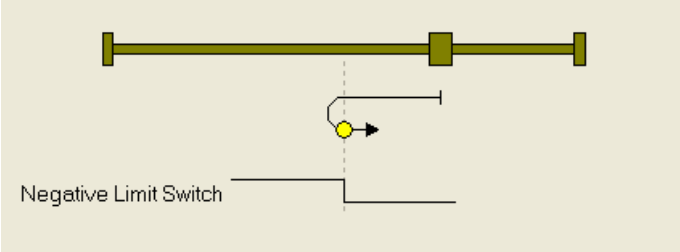
Type	Description	LED States	
		Green	Red
Bootloader	Bootloader is idle; waiting for firmware update.	Blinking at 90% duty cycle at about 1Hz	OFF
	Bootloader is working; firmware burn is in process.	Blinking at about 5Hz	OFF
	Firmware checksum error.	ON continuously	Blinking at 10% duty cycle at about 1Hz
	Bootloader checksum error.	ON continuously	Blinking at about 5Hz
	System error. An error has occurred during a firmware update procedure.	ON continuously	Blinking at about 1Hz
Firmware	Firmware is initializing.	Blinking at 10% duty cycle at about 1Hz	OFF
	Firmware is operational.	Blinking at 50% duty cycle at about 1Hz	OFF
	An error occurred during the firmware initialization. The firmware checksum calculation failed, or the FPGA initialization failed.	OFF	Blinking at about 1Hz

Axis Homing

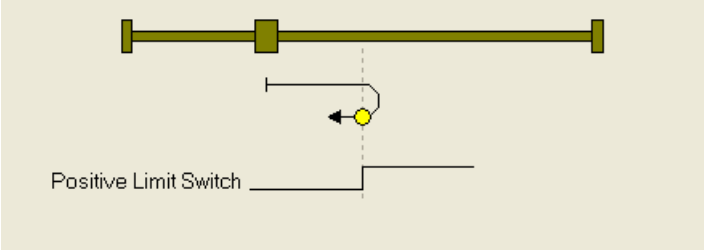
The homing procedure is the position initialization of a machine. Homing should be done at every machine startup. The MCHome Function block of the MotionPLCopen_SingleAxisMotion in the C&M application can be used to select and start one of the following homing methods. Connect the limit hardware switches to the selected axis inputs. Connect the home hardware switch to the Capture input.

The following DS402 specified homing methods are supported. Note that attempting to start a Homing Method other than what is listed in this document will be rejected by the firmware. Direction of motion is positive when moving from left to right. The yellow circle indicates the Homing event.

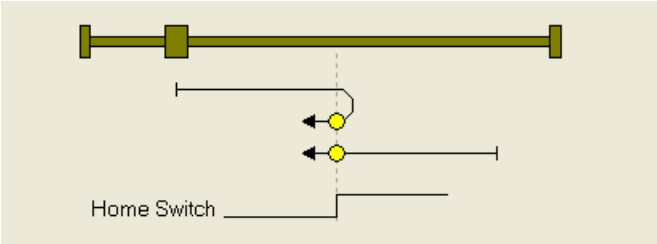
Homing Method 17
To use this method connect the Capture input directly to the negative limit switch.



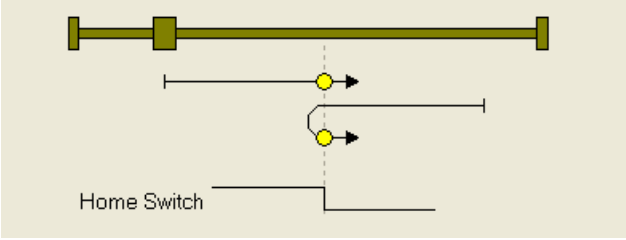
Homing Method 18
To use this method connect the Capture input directly to the positive limit switch.



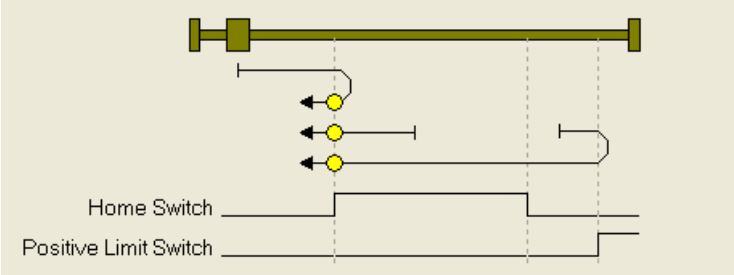
Homing Method 19



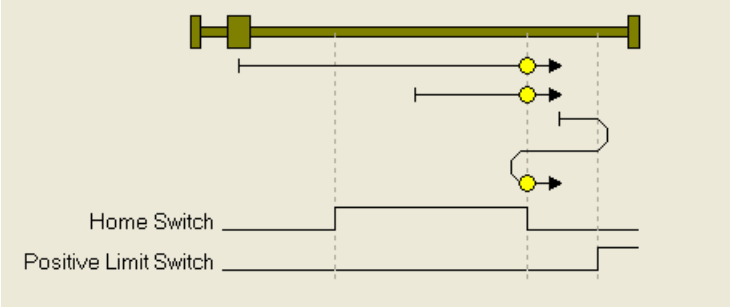
Homing Method 21



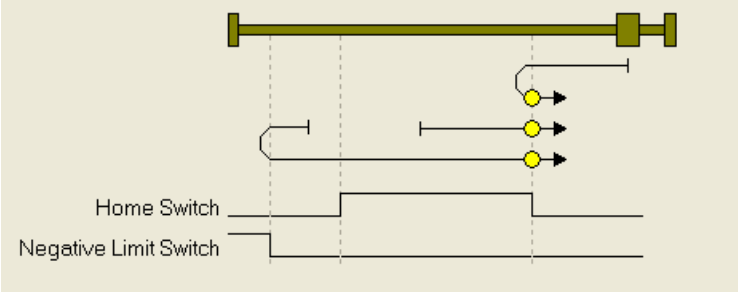
Homing Method 23



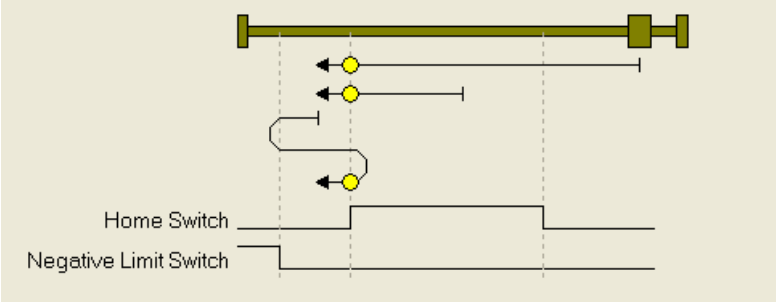
Homing Method 26



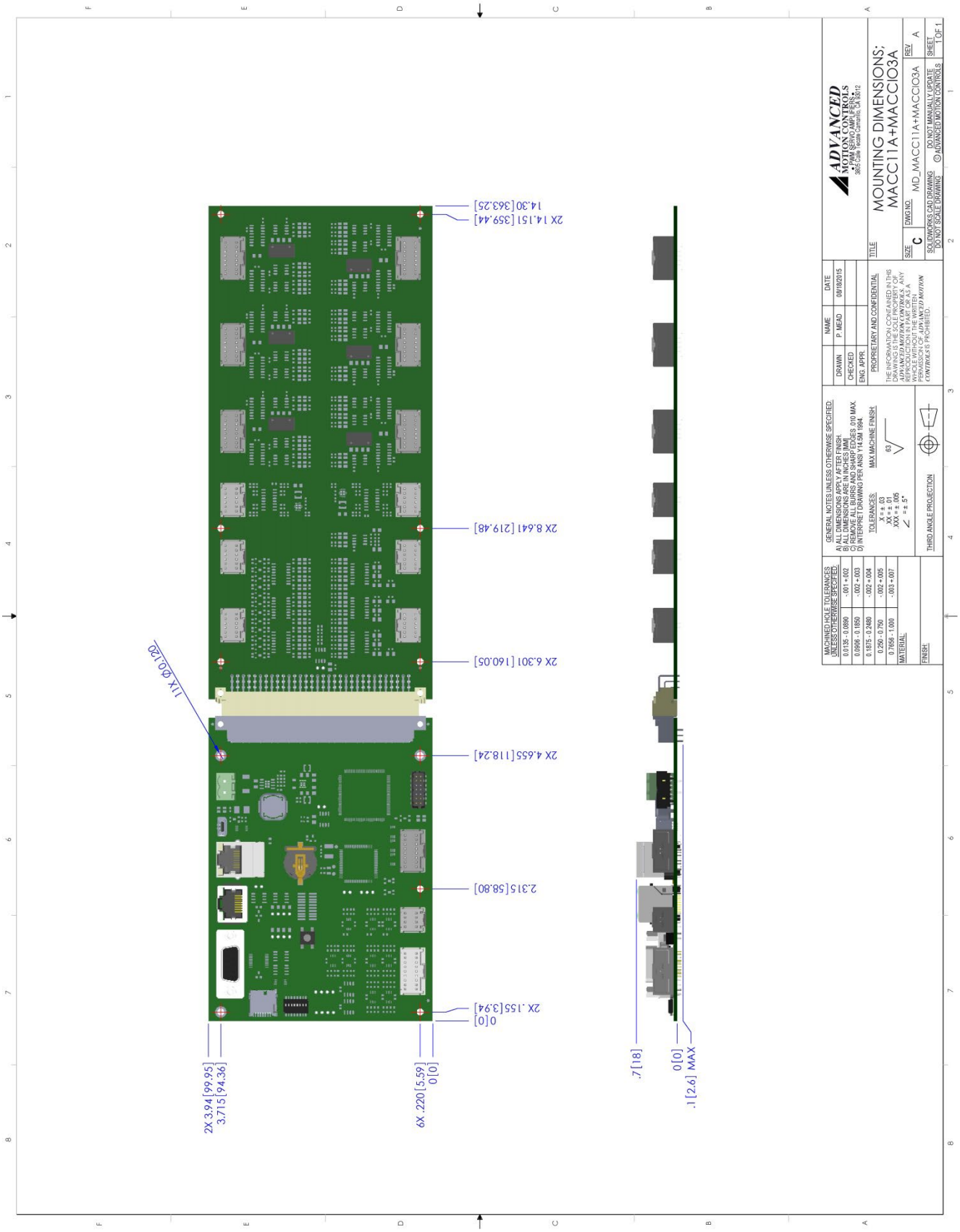
Homing Method 27



Homing Method 30



MACC11 and MACCIO3 Assembly Mounting Dimensions



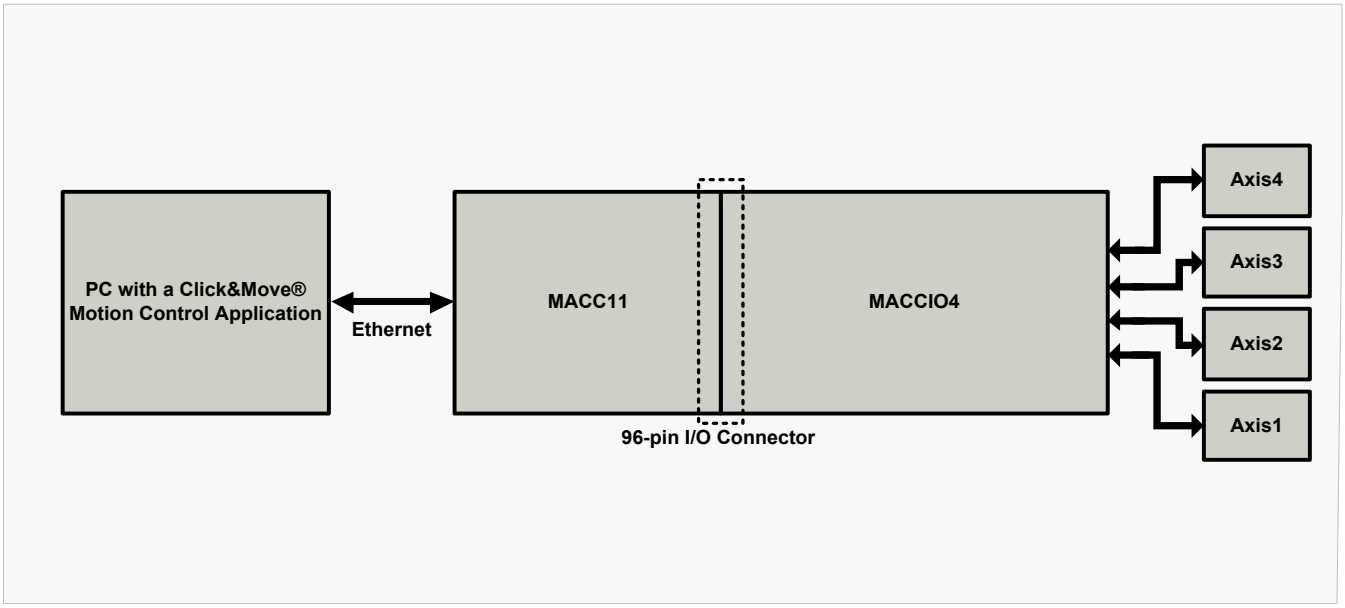
MACC11_1.1.1

This appendix contains information on the MACC11_1.1.1 firmware. It is compatible with the MACCIO4 I/O expansion module. For more information on the MACCIO4, refer to the "MACCIO Extension Boards" document. The primary function of the MACCIO4 is to allow support of position mode drives or stepper (open or closed loop configuration) using Step/Dir or PWM/Dir target position input with available Click&Move resources.

With this firmware, the MACC11 converts interpolated position target signals to Step/Dir or PWM/Dir signals in real time. From the motion control application point of view, the MACC11 acts as 4 independent CANopen based servo drives, featuring 4 independent CANopen object dictionaries including all the necessary CAN objects to simulate the functionality of 4 position mode servos. *ADVANCED* Motion Controls' analog and digital I/O are emulated as well, allowing the user access to the I/O resources of the MACCIO4 board. The Click&Move application can access the MACC11 using the Ethernet interface. The CanAdaptorEnetUdp CAN device option of the CAN_CHANNEL C&M function block encapsulates the CAN messages into UDP/IP frames that are decoded by the MACC11. The integrated PVT to discrete position algorithm uses the PVT points sent by the motion control application to generate an interpolated target position signal at 100μs update rate. The maximum pulse frequency is 1μs. The PWM frequency in PWM/Dir mode can be set between 100 Hz and 25500 Hz. The (CAN) device addresses of the emulated axes are constant (1 – 4). The IP address of the device and numerous other firmware parameters can be modified using a configuration tool.

This firmware version has the same functionality as the MACC11_1.0.2.

A typical system setup is shown below:



MACCIO4 Specifications

Mechanical Specifications		
Description	Units	Value
Size (H x W x D) [including MACC11]	mm (in)	219.48 x 99.95 x 18 (8.641 x 3.94 x 0.7)
Weight [including MACC11]	g (oz)	165 (5.8)
Operating Temperature Range	°C (°F)	0 - 75 (32 - 167)
Storage Temperature Range	°C (°F)	-40 - 85 (-40 - 185)
P1, P2, P3, P4 Motion Control Interface Connectors	-	12-pin, 2.00 mm spaced dual-row vertical header (Mating Connector Molex: 51353-1200)
P11, P12 Encoder Connectors	-	12-pin, 2.00 mm spaced dual-row vertical header (Mating Connector Molex: 51353-1200)

MACCIO4 Pin Functions

P1, P2, P3, P4 – Motion Control Interface Connectors*				
Pin	Name	MACCIO4 Name	Description / Notes	I/O
1	DIGITAL GROUND	GND	Digital Ground.	DGND
2	DIGITAL GROUND	GND	Digital Ground.	DGND
3	TRIGGER_AT_VALUE	OUTx_4	See Motion Control Interface Pin Details below	O
4	CAPTURE	INx_4	See Motion Control Interface Pin Details below	I
5	ENABLE	OUTx_3	See Motion Control Interface Pin Details below	O
6	FAULT	INx_3	See Motion Control Interface Pin Details below	I
7	OUT_PULLUP	OUT_PULLUPx	Digital output pull-up for the outputs**	-
8	DIGITAL GROUND	GND	Digital Ground.	DGND
9	DIR	OUTx_2	See Motion Control Interface Pin Details below	O
10	IN_n+1	INx_2	General purpose digital input***	I
11	STEP / PWM	OUTx_1	See Motion Control Interface Pin Details below	O
12	IN_n	INx_1	General purpose digital input***	I

*P1 = Axis1; P2 = Axis2; P3 = Axis3; P4 = Axis4; P9 = Axis5; P10 = Axis6
**P1/P2 and P3/P4 have common PULLUP signals.
***The system wide 8 available GPIN signal numbering is as follows: P1=1,2; P2=3,4; P3=5,6; P4=7,8

Motion Control Interface Pin Details

All signals of the motion control hardware interface are non-isolated single-ended signals. The hardware interface to the position mode drives or steppers contains the following signals:

Signal	Description
Step Output	Every pulse on this output increments/decrements the position counter of the positioning device.
PWM Output	When PWM/Dir mode has been selected, this is the PWM signal output.
Dir Output	Direction signal for the device. The level of this signal indicates if the position counter should be incremented or decremented at every Step pulse.
Enable Output	Enables or Disables the device.
TriggerAtValue Output	Programmable firmware function. A comparator implemented in the FPGA can be set up to compare some selectable internal signals (available inside the FPGA) of the emulated drive. The TriggerAtValue Output indicates when the preset value and the signal are the same. The use of this signal is application specific.
Ready or Fault Input	Indicates the internal status of the positioning device. When active (or inactive if the polarity is inverted) the status word of the emulated servo drive will indicate a “Drive Internal Error” to the motion control application. Default polarity is INVERTED, meaning by default the input acts as a Ready status indicator
Capture Input	Selectable signals from the emulated drive can be captured using the selected edge of the Capture Input. Only signals that are accessible inside the FPGA can be captured. This can be used as a home switch input, capturing the actual position (always equal to the target position in the MACC11) during the homing procedure.

The MACCIO4 has support for up to four quadrature encoder inputs that can be used as the position signal source or handwheels.

P5 – Encoder Connector			
Pin	Name	Description / Notes	I/O
1	GROUND	Ground	GND
2	GROUND	Ground	GND
3	ENC_B_2-	Differential encoder 2 B-channel negative input (leave open for single-ended encoders)	I
4	ENC_B_1-	Differential encoder 1 B-channel negative input (leave open for single-ended encoders)	I
5	ENC_B_2+	Differential encoder 2 B-channel positive input	I
6	ENC_B_1+	Differential encoder 1 B-channel positive input	I
7	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
8	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
9	ENC_A_2-	Differential encoder 2 A-channel negative input (leave open for single-ended encoders)	I
10	ENC_A_1-	Differential encoder 1 A-channel negative input (leave open for single-ended encoders)	I
11	ENC_A_2+	Differential encoder 2 A-channel positive input	I
12	ENC_A_1+	Differential encoder 1 A-channel positive input	I

P6 – Encoder Connector			
Pin	Name	Description / Notes	I/O
1	GROUND	Ground	GND
2	GROUND	Ground	GND
3	ENC_B_4-	Differential encoder 4 B-channel negative input (leave open for single-ended encoders)	I
4	ENC_B_3-	Differential encoder 3 B-channel negative input (leave open for single-ended encoders)	I
5	ENC_B_4+	Differential encoder 4 B-channel positive input	I
6	ENC_B_3+	Differential encoder 3 B-channel positive input	I
7	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
8	+5V OUT	+5V encoder supply output. Maximum load on pins 7 and 8 together is 500mA.	O
9	ENC_A_4-	Differential encoder 4 A-channel negative input (leave open for single-ended encoders)	I
10	ENC_A_3-	Differential encoder 3 A-channel negative input (leave open for single-ended encoders)	I
11	ENC_A_4+	Differential encoder 4 A-channel positive input	I
12	ENC_A_3+	Differential encoder 3 A-channel positive input	I

Configuration Program

The MACC11_1.1.1 firmware has a common configuration program with the MACC11_1.0.2 firmware. All the behaviors described in the MACC11_1.0.2 Configuration Program description apply for use with the MACC11_1.1.1. The unavailable axes and features will be disabled when the configuration program with the MACC11_1.1.1 firmware.

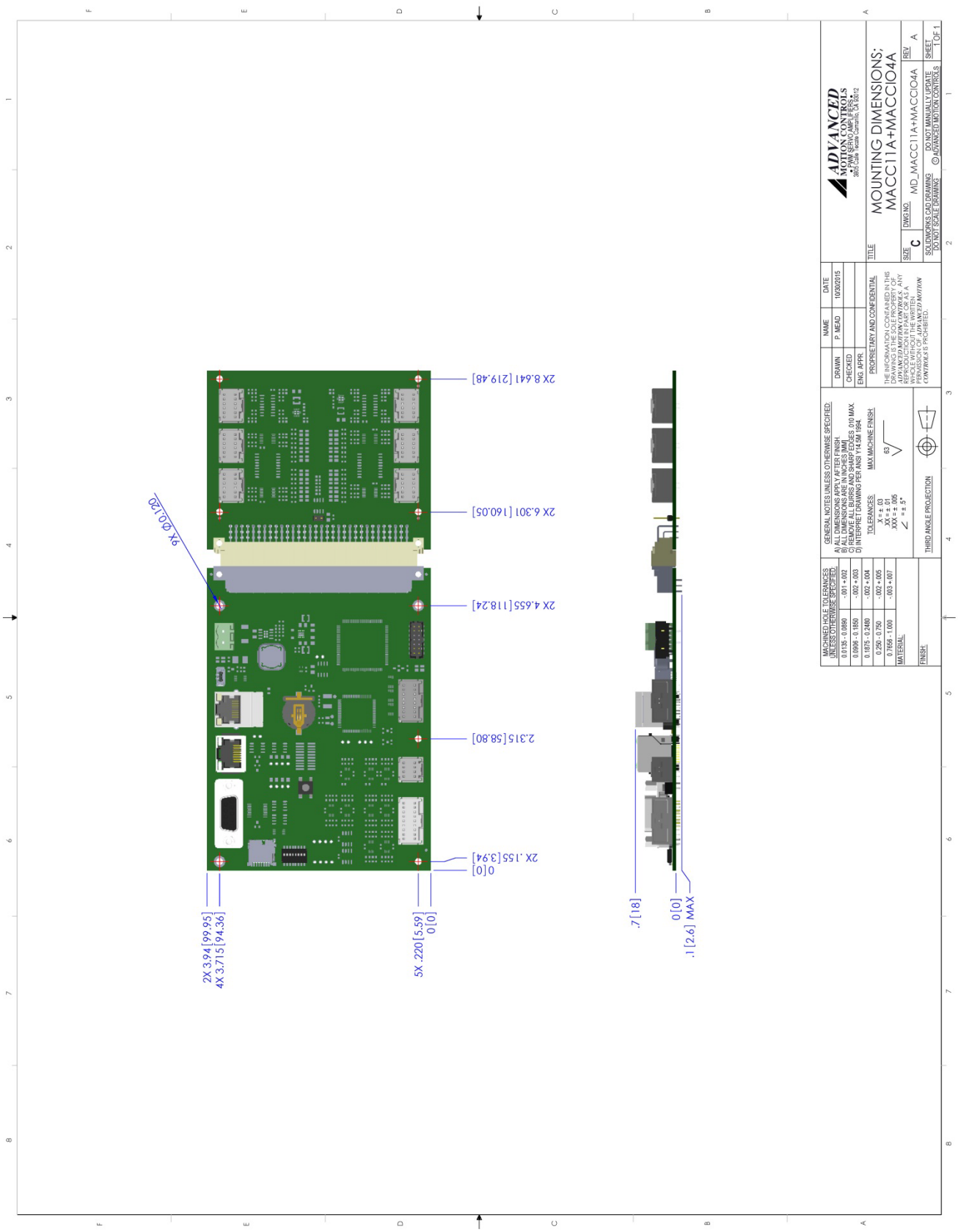
Status Indicators

Refer to the MACC11_1.0.2 firmware description for more information.

Axis Homing

Refer to the MACC11_1.0.2 firmware description for more information.

MACC11 and MACCIO4 Assembly Mounting Dimensions



CUSTOMIZATION INFORMATION

ADVANCED Motion Controls also has the capability to promptly develop and deliver specified products for OEMs with volume requests. Our Applications and Engineering Departments will work closely with your design team through all stages of development in order to provide the best servo drive solution for your system. Equipped with on-site manufacturing for quick-turn customs capabilities, *ADVANCED* Motion Controls utilizes our years of engineering and manufacturing expertise to decrease your costs and time-to-market while increasing system quality and reliability. Feel free to contact Applications Engineering for further information and details.

Examples of Customized Products

- Optimized Footprint
- Private Label Software
- OEM Specified Connectors
- No Outer Case
- Increased Current Resolution
- Increased Temperature Range
- Custom Control Interface
- Integrated System I/O
- Tailored Project File
- Silkscreen Branding
- Optimized Base Plate
- Increased Current Limits
- Increased Voltage Range
- Conformal Coating
- Multi-Axis Configurations
- Reduced Profile Size and Weight